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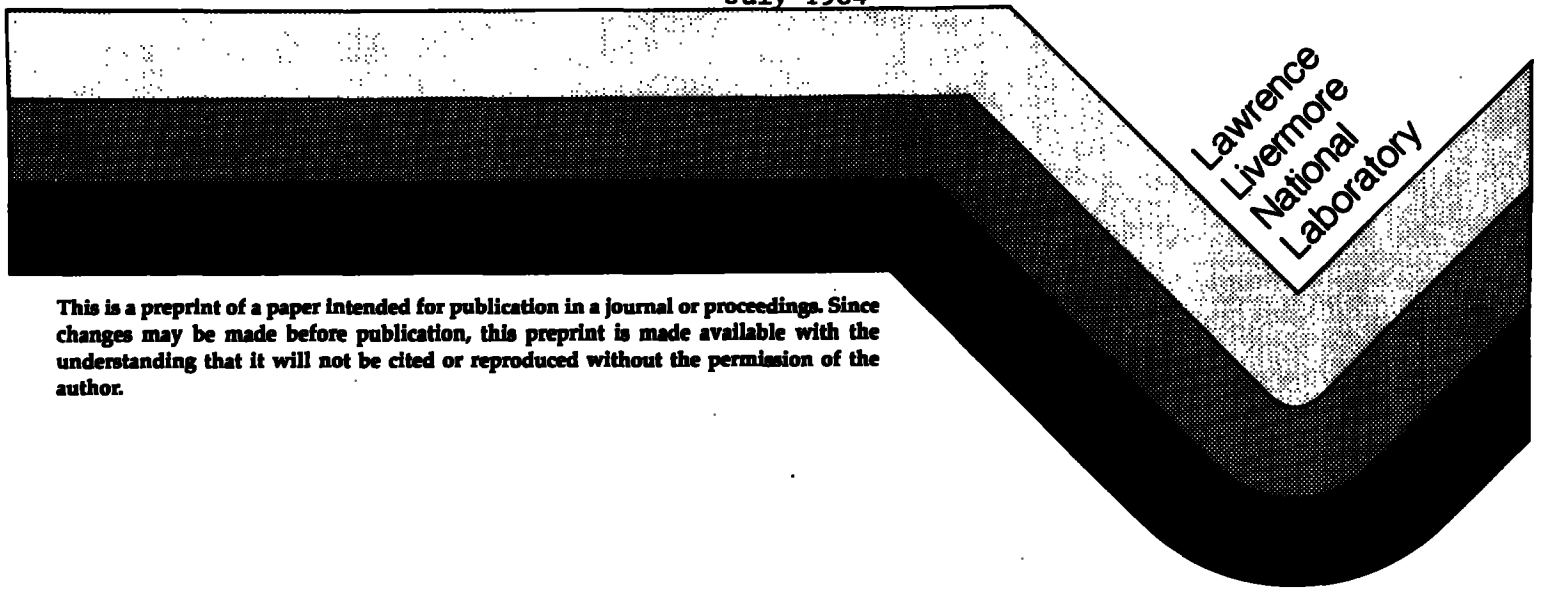

DISCLAIMER

POWER MOS FAST SWITCHING TECHNIQUES*

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Summary

High voltage, high peak power pulse generation has depended strongly on non solid-state switching technology when speed and voltage requirements are respectively less than a few nanoseconds and greater than a few hundred volts. Switching of greater than 10 kilowatts in less than three nanoseconds, for example, limits the designer to only a few technologies, none of them particularly simple or inexpensive. The addition of high rep-rate requirements compounds the problem, and will generally limit the designer to a hard tube approach if the rep rate and/or risetime are outside available thyratron envelopes.

The emergence of power metal oxide semiconductor field effect transistors (power MOS) over the past few years has created a revolution in the design of mass produced circuits such as switching power supplies. Their switching speed of 20 to 50 nanoseconds in these applications is an order-of-magnitude improvement over bipolar types. We have examined the inherent switching speed limitations of this technology and we have discovered that, using appropriate and reasonably simple techniques, power MOS is a powerful medium for implementation of high power pulse generators with switching times approaching one nanosecond.

We have experimentally obtained switching speeds of 1.3 nanoseconds under lightly loaded conditions (400 volts into 50 ohms) and single device peak currents of 145 amperes in approximately five nanoseconds. We have just begun this development and have identified several obvious improvements which should make our approach even more versatile and useful in the future.

Background

The emergence of power MOS in the past few years has solved many power circuit implementation problems and created a new generation of small, lightweight high frequency switching power supplies. This regime is far removed from the smaller domain of high voltage pulse generators requiring output voltages of up to 10 kV and with risetime requirements sometimes below one nanosecond. Such pulsers find use as Pockels cell drivers in laser systems, microchannel plate gates, rf modulators, other sensor drivers and a variety of other miscellaneous tasks continually emerging in the scientific community.

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The key element in a pulse generator circuit is the switch, and several technologies have been available for fast, high voltage applications in the past. For work under five nanoseconds, the choices are somewhat limited. Gas switches (spark gaps) and krytrons have been popular as high performance, low cost approaches. Their use is often precluded, however, by jitter and life problems. More recently, the bulk semiconductor photoconductive (Auston) switch has emerged[1] as an effective high voltage switch, but requires a complex pulsed laser system for turn-on. Also on the horizon is the electromagnetic shock line[2], but pulse shape is difficult to control with this device and an active input driver must be provided. Avalanche transistors continue to be used and indeed present an attractive solution to many engineering problems. They are, however, peak power limited and often exhibit reliability problems. Such difficulties are compounded when devices are stacked to attempt to circumvent the peak power issue. For completeness, the hydrogen thyratron is mentioned, but is risetime limited to around three nanoseconds[3]. Most thyratrons are no faster than 15 nanoseconds.

This often leaves the vacuum tube as the only viable switching element available for under three nanosecond, greater than 10 kW, rep-rated circuit requirements requiring low jitter. Such specifications describe a useful Pockels cell driver, for instance. In this speed regime component selection is generally limited to microwave planar triodes such as the Varian/Eimac Y-690[4]. High-speed circuits implemented with these devices tend to be complex because the Miller effect of the triode (no comparable tetrodes are available) limits power gain and the cathode current for pulse applications is limited to around 12 amperes/cm^2 in practical implementation where rep-rated reliability is a concern.

Device Development

The emergence of MOS as a candidate started with others[5]. All power MOS is implemented as an array of thousands of tiny cells on each transistor chip, so the switching speed inherent in any cell is very fast. Figure 1A depicts a simple equivalent circuit of a conventional MOS transistor, showing those equivalent elements which limit device switching speed. The key switching problem is charging the gate-source capacitance of each cell somewhat faster than the desired output switching speed.

Given an ideal step generator, e_p, there remain several circuit elements impeding rapid turn-on (or turn-off, a highly desirable feature only shared with the vacuum tube in this speed/power regime). One must charge gate-source capacitance C_{iss} and the smaller drain-gate reverse capacitance C_{rss}, the latter's significance being multiplied by the Miller effect

while the transistor is in its active region. Obviously the source impedance of the generator must be sufficiently low. Lumped into R_G is also the resistivity of the gate interconnection on the chip itself, which may be significant with some product lines.

Using devices in conventional packages such as the TO-220, one is limited as to control of inductances L_G and L_S. The value of each is on the order of 10 nanohenries using the TO-220 package in a tight circuit configuration. L_S is particularly degrading because, as the device turns on, an $L_S di/dt$ term is impressed on the source with respect to the ground indicated in Figure 1A. This subtracts from the ground referenced gate drive, e_p and results in a delaying step in the drain falltime.

It is possible to partially circumvent these charging limitations with conventional packages by overdriving the gate. We found, for instance, that the Intersil IVN6000CNU type will generally withstand a gate-source stress of 100 volts and we were able to switch 300 volts into 30 ohms in approximately three nanoseconds using this approach. We would limit such overstressing techniques to information gathering circuit experiments where reliability and reproducibility are not issues, however.

A more rigorous and versatile method of attacking the problem is to repackage the transistor chips in a manner which meets our special requirements. This is depicted schematically in Figure 1B. Through the use of a microwave stripline transistor style package and multiple bond wires from chip to package lead connections, we can address inductances L_G, L_D', L_D' and L_S'. An important further change is the addition of a second source lead with inductance L_S'', reserved for a floating gate drive. This is implemented by an extra set of bond wires to the transistor chip and an extra package lead. Except for the common inductance on the chip itself, this decouples the $L_S' di/dt$ term from the gate drive.

We polled vendors of microwave style transistor packages seeking a large chip mounting cavity, wide stripline style leads, and the willingness to add a custom lead for the second source connection. We selected the Kyocera International, Inc. KMC-19629 package and ordered a number of units, as shown in Figure 2.

We also spoke with a number of power MOS vendors, particularly with Intersil, Inc. and International Rectifier, Inc., and selected the latter's IRFC440 chip as most suitable for our needs. This device is designed to operate at a higher current density than previous IR type and hence has a lower ratio of input capacitance to on resistance. Rated voltage is 500 volts. In talking to the manufacturers, it became clear that joule heating of the chip during the pulse was the only significant damage related limitation to device current handling capability.[6,7] Device data sheets typically give a factor of four higher than dc current limitation for pulse operation, but this is a somewhat artificial limit tailored for the "slow" power supply designer and unnecessarily pessimistic for fast pulses less than 50 nanoseconds in duration. A harder limit is the increase in r_{ds} with increasing drain current; data sheets may be extrapolated to estimate this or special device testing independently carried out.

We discovered that two of these chips would fit nicely in the Kyocera package, forming a hybrid circuit with twice the current handling cap- ability. The inherent current sharing feature of MOS makes paralleling possible without elaborate precautions. Chip mounting and bonding was carried out by Los Alamos National Laboratory, with 10, two mil wires going from each bonding pad to the appro- priate package terminal. Chip pad areas are ample for even the twenty individual bonding wires for the dual source connection, as shown in Figure 2.

Circuit Development

The two IRFC440 chips mounted together in our single package have a joint C_{iss} of approximately 3000 pf. If we wish to impress a gate-source voltage, V, on the devices in a period, T, of one nanosecond, the average charging current, $C_{iss}V/T$, equals 10 amperes. Alternatively, The required source impedance, R_G, is on the order of T/C_{iss}, or 0.3 ohms. The gate drive circuit therefore represents a major challenge. The power output circuit might take on a number of forms, depending on application. We have accomplished our testing using simple resistive loads of 50 ohms and less in order to characterize performance. Tight circuit layout is obviously critical, with a low inductance ground plane necessary along with wide, short interconnects to minimize circuit inductance.

After some effort, we have developed the gate drive circuit of Figure 3. This embodiment provides a drive signal swing from zero to +25 volts, with the critical +4 to +10 volt transition taking place in 0.8 nanoseconds, when driving the 3500 pf gate-source load (Figure 4). The driving tran- sistors are high frequency devices in stripline packages normally used in communications equip- ment. The circuit provides a zero volt level for FET turn-off. A symmetrical, $\pm$15 volt swing around the gate-source threshold voltage of approximately + 4 volts might provide more effective turn-off, but this additional complexity was not implemented.

Experimental Performance

Figure 5 shows the drain waveform achieved with a 50 ohm load using two IRFC440 chips in parallel in a single Kyocera package as previously discussed. When corrected for the 1.5 nanosecond risetime of the instrumentation used, a 90-10 percent falltime of 1.3 nanoseconds or less has been obtained. Peak current handling capability was explored by reducing the load resistor to 0.6 ohms (including CVR). Figure 6 shows the current waveform, with a 10-90 percent risetime to 108 amperes in approximately five nanoseconds. Performance was evaluated with drain currents to 145 amperes (obtained by raising the drain voltage from 400 to 500 volts). Fall times were only slightly slower at the higher current level.

In order to determine the effectiveness of the new package, test were conducted with two, paralleled IRF840 transistors substituted in the

circuit. Each of these devices consists of an IRFC440 chip in a TO-220 plastic package. A load resistance of 10 ohms was selected for this test as an intermediate between the loadings used in initial testing. Similar data was taken on the original circuit. It was found that the custom package yielded a factor of two in switching speed (1.9 vs. 4.9 nanoseconds). The corresponding drain currents were also measured. These data are reduced in figure 7, where they are plotted as on resistance as a function of time for the two different transistor types. An aside of this development is, while the special packaging results in greatly improved performance, robust gate drive on the standard, inexpensive TO-220 devices can produce impressive results, also.

Proposed Improvements

During the course of testing, several areas capable of improvement were noted. Most concerned reduction of circuit inductance. Design of an even lower inductance transistor package is in work at LANL. More careful circuit layout appears to be in order, also. The subohm, subnanosecond gate drive requirements present some interesting challenges to both the circuit designer and packaging engineer.

Emerging higher voltage devices also promise higher power levels and higher output voltages without stacking or use of transformers. We are presently preparing to test developmental Motorola 850 volt devices in our package and we have 1000 volt components on order.

We are also investigating techniques for adding of pulse outputs, either by a transformerless stack ing arrangement (which presents obvious gate drive problems) or by use of transformers. It is reasonable to expect that the several kilovolts required to drive Pockels cells, for instance, could be implemented using this approach and at a cost comparable to or less than existing hard tube, thyratron or spark gap based drivers.

Based on our relatively brief experience in this medium, we predict single device maximum currents of 200 amperes, risetimes less than one nanosecond and voltage holdoff ability of at least one kilovolt when the technology matures. Allowable repetition rates are circuit dependent, but could be in the several megahertz range. Such performance is assumed to be within the realm of available (or soon to be available) device voltage and chip dissipation limitations and should be suitable for reliable circuit performance in mass produced equipment.

Conclusions

It has become apparent that the power MOS approach is competitive with planar triodes in terms of speed, power handling capability, jitter and cost for many applications. The lifetime, ruggedness, size and reliability advantages normally attributed to solidstate circuitry make this new approach particularly attractive. We expect usage to spread to many fast pulse areas as experience accumulates.

Acknowledgments

We would like to thank Mr. Steve Davis, formerly with Power Spectra, Inc., San Leandro, CA and Mr. Steve Clemente of International Rectifier for their guidance which inspired this development.

It is emphasized that evaluated devices were selected on the basis of preliminary studies and that other manufactuer's products meeting the requirements herein should perform equally well.

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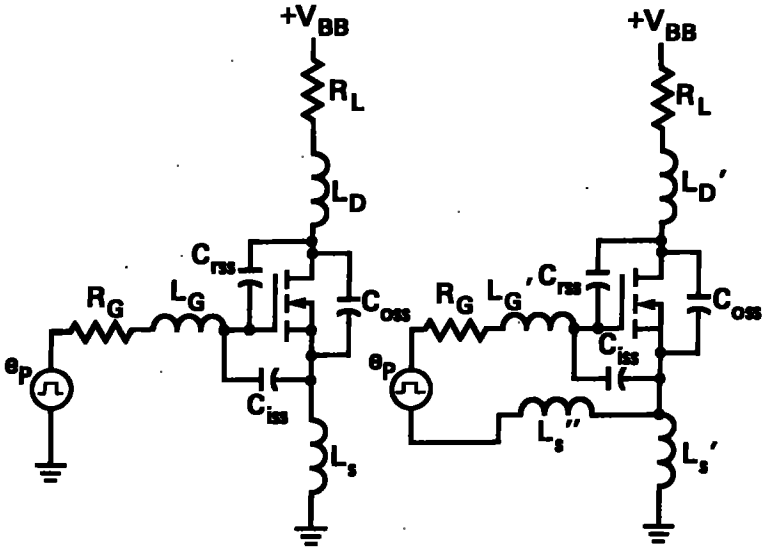


Conventional circuit
Figure 1A

Special packaging
Figure 1B

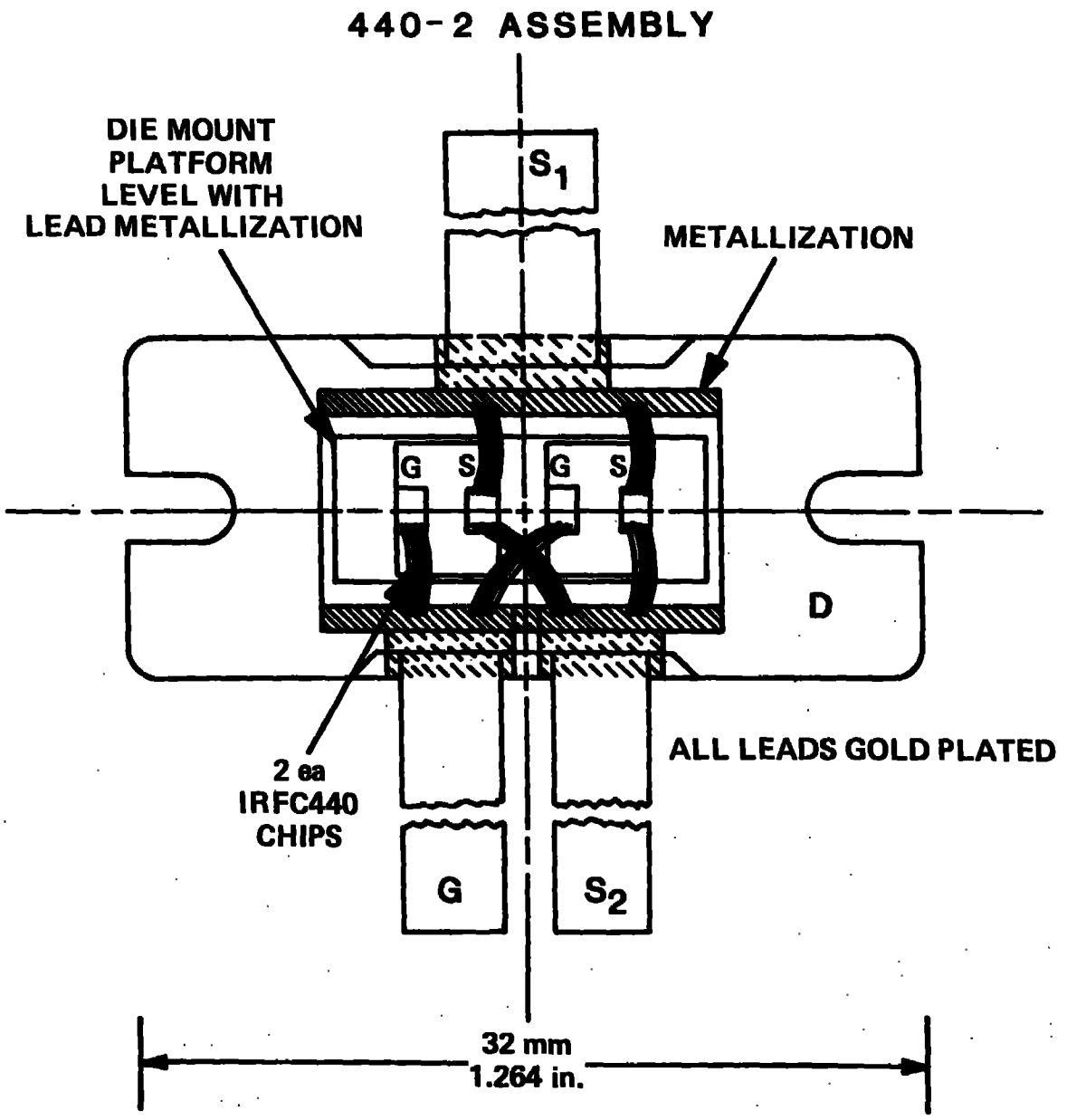
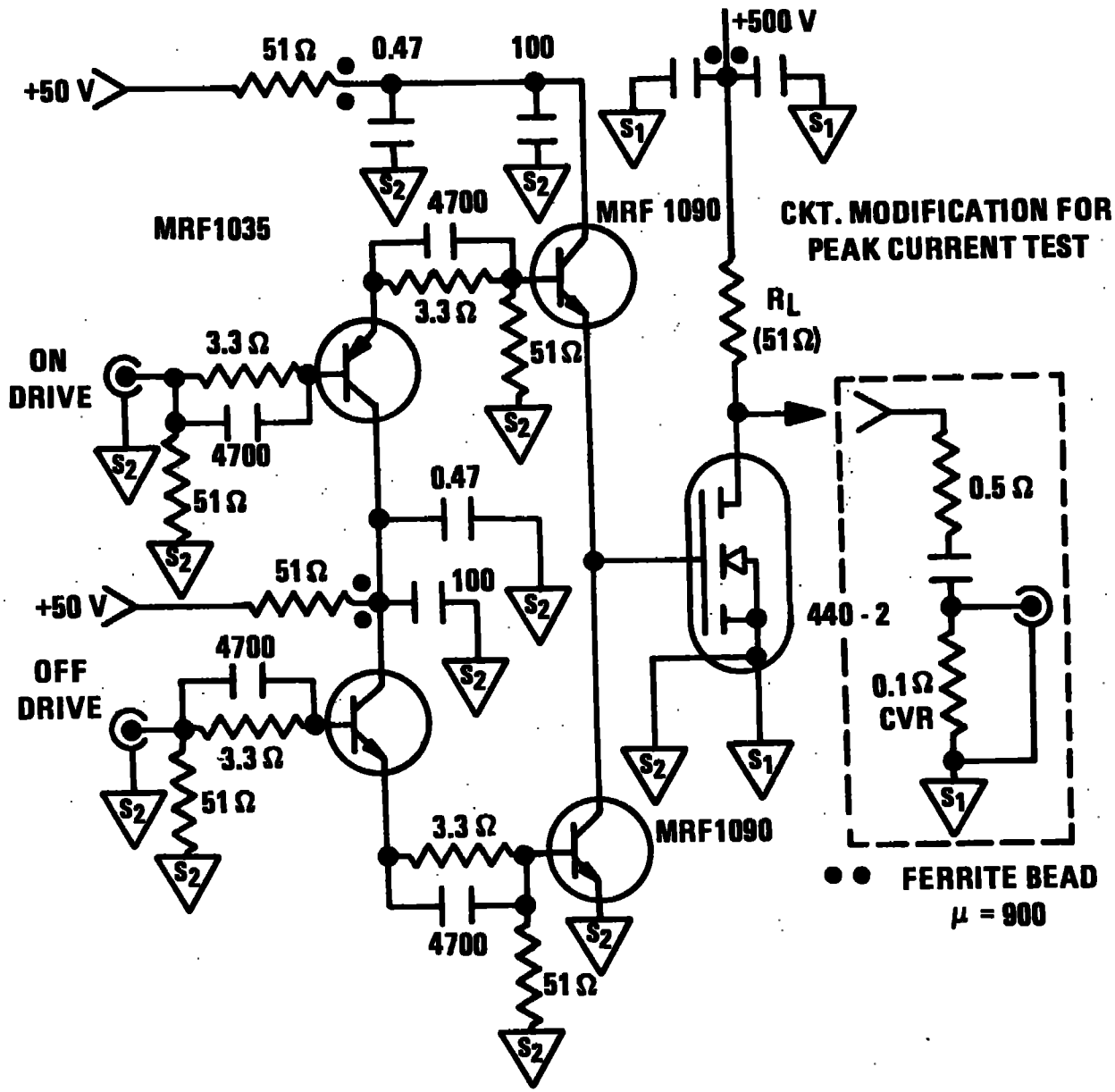

440-2 ASSEMBLY
DIE MOUNT PLATFORM LEVEL WITH LEAD METALLIZATION
METALLIZATION
S_1
G
S
G
S
D
2 ea IRFC440 CHIPS
ALL LEADS GOLD PLATED
G
S_2
32 mm
1.264 in.

FIGURE 2



GATE DRIVE CIRCUIT
FIGURE 3

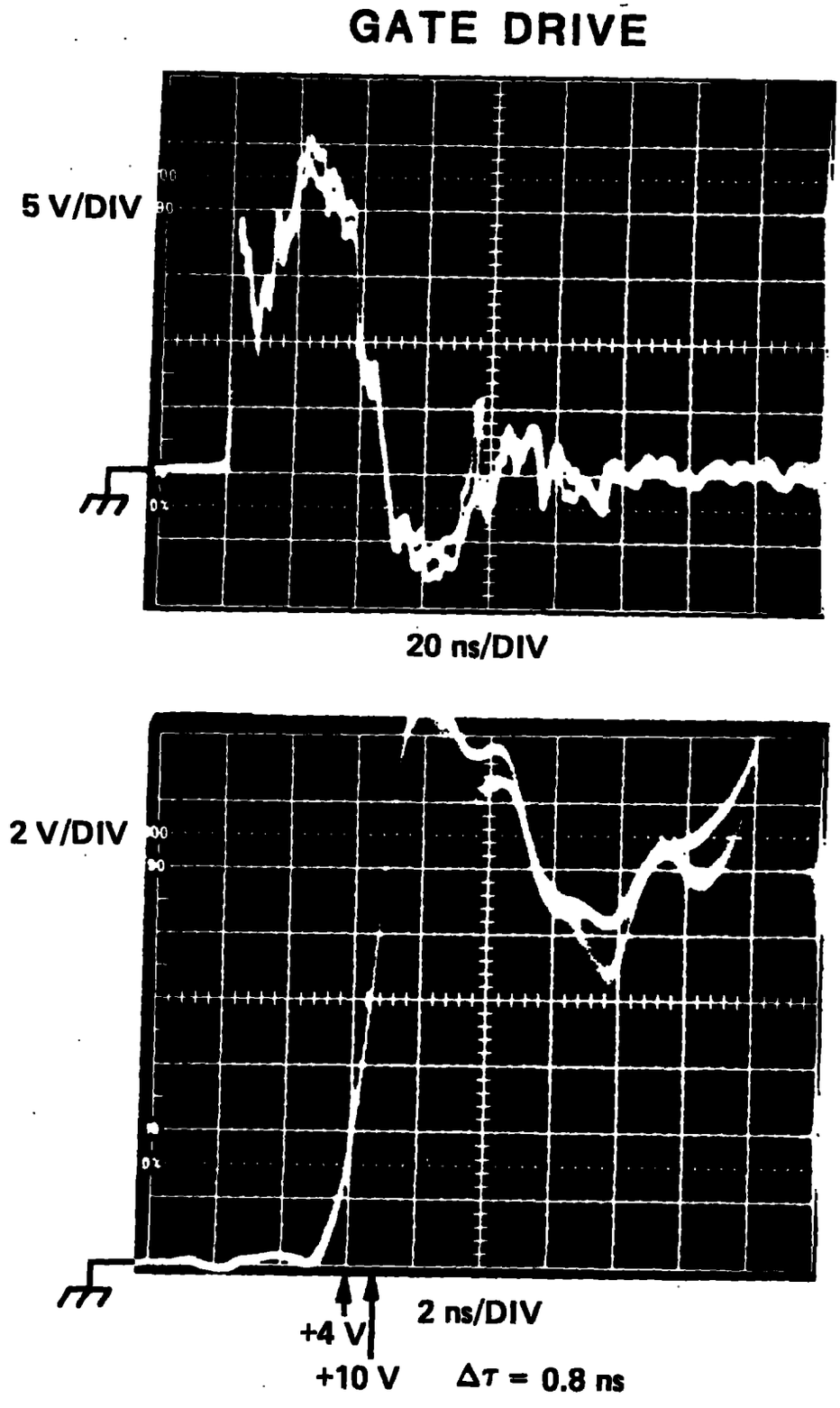
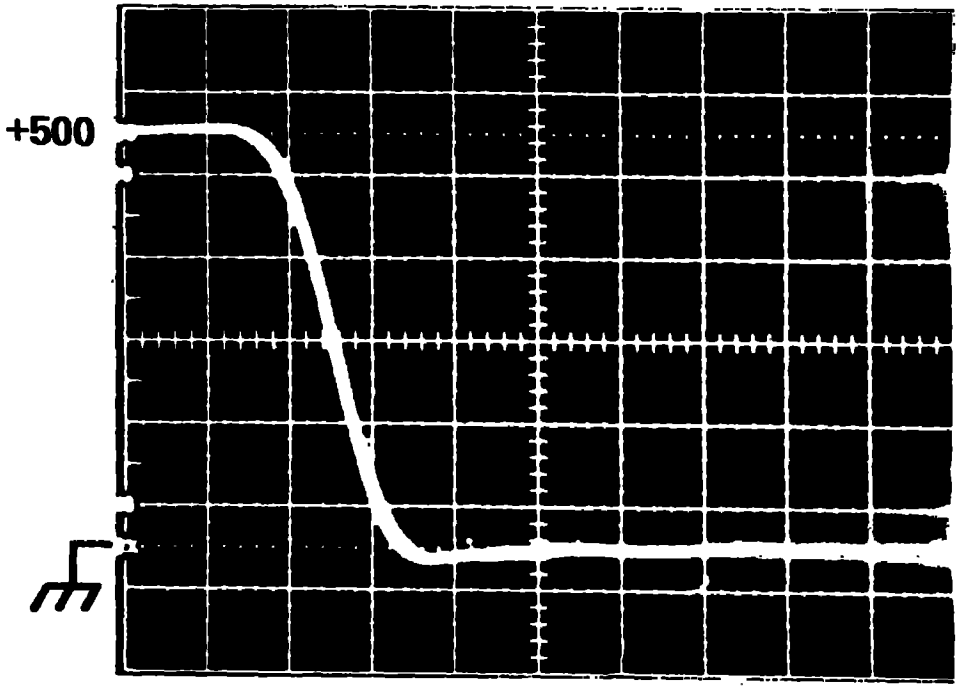


FIGURE 4

VOLTAGE FALL



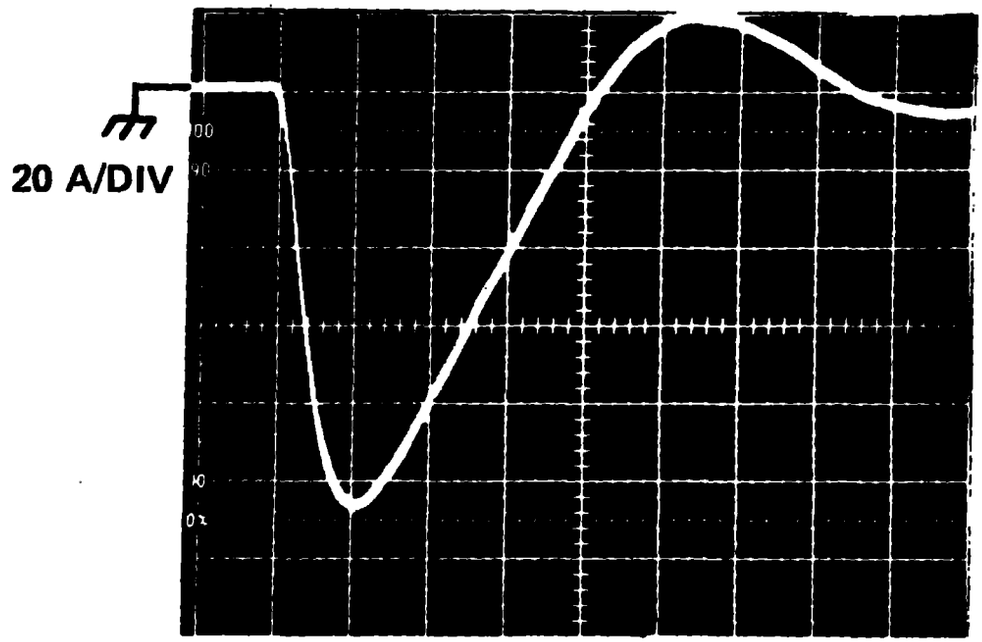
τ_f = 2 ns

2 ns/DIV

τ_f (SCOPE + PROBE) = 1.5 ns = > CORRECTED FALL TIME τ_{fc}

τ_{fc} = 1.3 ns

FIGURE 5



PEAK CURRENT
FIGURE 6

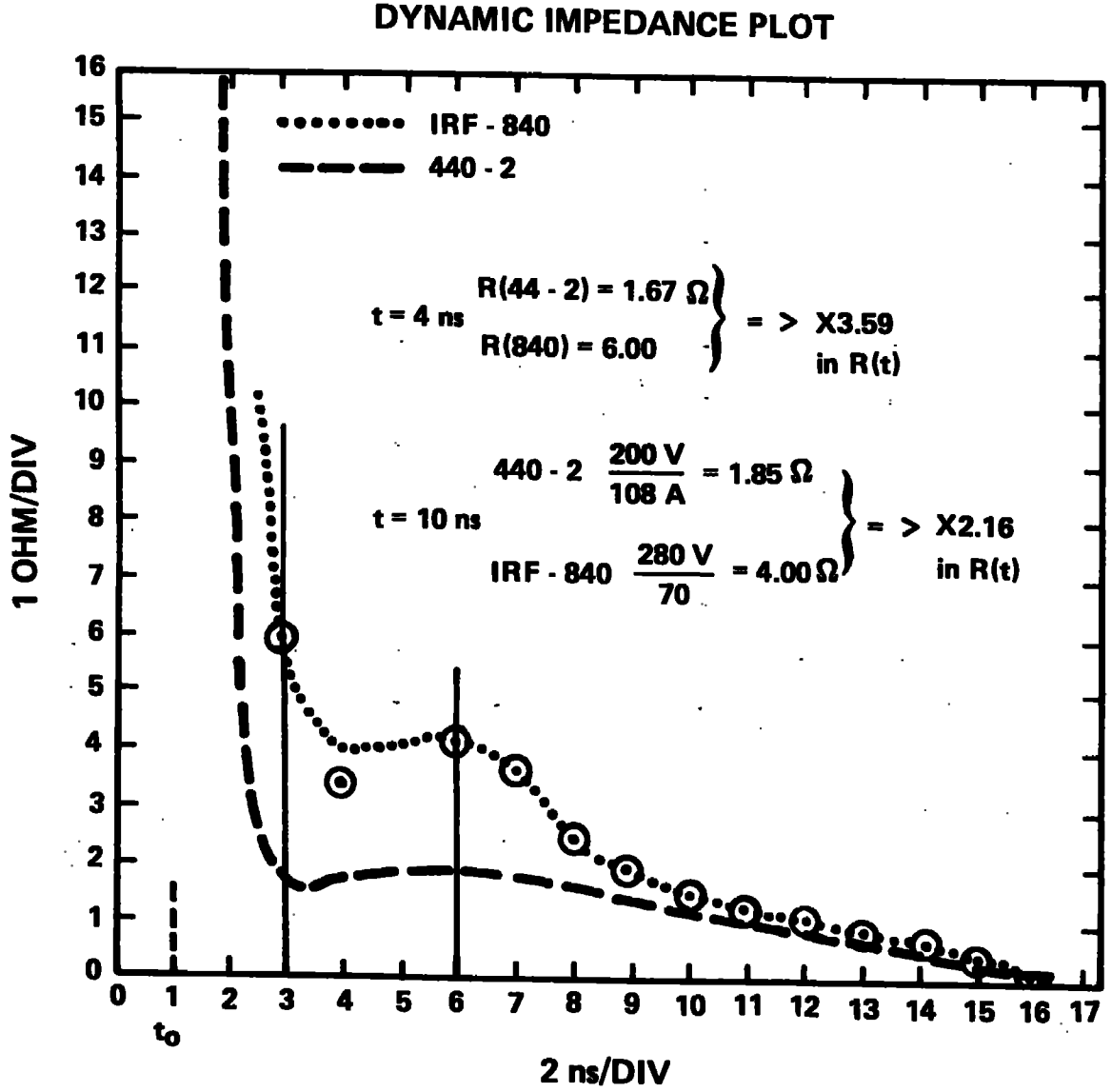

DYNAMIC IMPEDANCE PLOT
IRF - 840
440 - 2
t = 4 ns
R(44 - 2) = 1.67 Ω
R(840) = 6.00
= > X3.59
in R(t)
t = 10 ns
440 - 2 200 V / 108 A = 1.85 Ω
IRF - 840 280 V / 70 = 4.00 Ω
= > X2.16
in R(t)
1 OHM/DIV
2 ns/DIV
t_o

FIGURE 7